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PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Serial No:	10/705,386	Docket No:	2011137
Filing Date:	11/10/2003	Applicant:	Pierre Liu
Examiner:	VU, QUANG D	Art Unit:	2811
Title:	INTEGRATED CIRCUIT PACKAGE		

To: Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

TRANSMITTAL OF AMENDMENT

1. Transmitted herewith is a response to an office action for this application prepared and submitted by the Applicant.

2. Applicant is entitled to Small Entity Status.

3. The proceedings herein are for a patent application and the provisions of 37 CFR 1.136 apply. Applicant believes that no extension of time is required. However, a conditional petition is hereby made to provide for the possibility that applicant has inadvertently overlooked the need for a petition for extension of time.

4. No fee is required at this time.

5. Certificate of Mailing (37 CFR 1.8a): I hereby certify that this paper (along with any referred to as being attached or enclosed) is being deposited with the United States Postal Service on the date shown below with sufficient postage as First Class Mail in an envelope addressed to: Mail Stop Non-Fee Amendment, Commissioner for Patents, P.O. Box 1450, Arlington, VA 22313-1450.

Respectfully submitted,

Date: May 24, 2005

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To:	THE ASSISTANT COMMISSIONER FOR PATENTS Washington, D.C. 20231		

RESPONSE TO OFFICE ACTION

Dear Sir:

In response to the Office Action dated 03/25/2005, Applicant submits the following arguments.

ARGUMENTS

1.Claims 1-4 are rejected under 35 USC §102 (b) as being anticipated by US patent NO.6,048,755 to Jiang et al.

Applicant thinks that it is true that Jiang does not disclose that an integrated circuit package has resistant layer located on the lower surface of the substrate, and is located between the long slots 56 and wiring region 58. Therefore, while the flowed glue of the glue layer 44 is flowed to lower surface 54of the substrate 40 through the long slot 56, the flowed glue can be prevented by the resistant layer 42 to flow to the wiring region 58, so that the connected points 60 may not covered by the flowed glue.

According to the examiner's opinion, please refer to the 755,patent, which is shown a method for fabricating a BGA package, the method includes the step of providing a substrate having a first surface with a pattern of conductor s thereon, and an opposing second surface with a die attach area thereon. A first solder is formed on the first surface with via opening to ball bonding pads on the conductors. A second solder mask is formed on the second surface with an opening on the side die area. The opening in the second solder mask permits a die

to be placed through the opening and adhesively bonded directly to the substrate. The die can then be wire bonded to the conductors and encapsulated in an encapsulating resin. In addition solder balls can be placed in the via openings and bonded to the ball bonding pads.

The invention has the following advantages.

1. Since if the flowed glue of the glue layer44 is flowed to the lower surface54 of the substrate40 through the long slot56, the flowed glue can be prevented by the resistant layer42 to flow to the wiring regions58, thus, the connected points60 can be not covered by the flowed glue.

2. Since the length of the wiring regions58 are shorter than the long slot56, so that, while drilled the long slot56, if the substrate40 is cracked, which is can be not coupled to the wiring regions58,thus the connected points60 can be not covered by the flowed flue of the glue layer44

Thus, the Jiang does not disclose a similar structure to that of this application, and does not motivate the Applicant to finish this application. Reconsideration of the Claims 1 - 4 is politely requested.

In light of the above remarks, Applicant now asserts that all of the grounds for rejection have been traversed or overcome by the detailed arguments, and that all of the present claims are in condition for immediate allowance. Applicant therefore requests reconsideration of the rejections, and solicits allowance of the present claims at an early date.

Thank you for your consideration.

Respectfully submitted,

Date: 5/20/2005 Jichen WU

Jichen WU

Title of Officer: Manager of Kingpak Technology Inc., the Assignee of this application

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